



### Identification

DTM63391B 128Mx72  
1GB 1Rx8 PC2-5300E-555-12-F0

### Performance range

Clock/ Module Speed/ CL-t<sub>RCD</sub> -t<sub>RP</sub>  
333MHz/PC2-5300/ 5-5-5  
267MHz/PC2-4200/ 4-4-4

### Features

240-pin JEDEC-compliant DIMM, 133.35 mm wide by 30 mm high

Operating Voltage: 1.8 V  $\pm$ 0.1

I/O Type: SSTL\_18

Data Transfer Rate: 5.3 Gigabytes/sec

Data Bursts: 4 or 8 bits, Sequential or Interleaved ordering

Programmable I/O driver strength (OCD)

Programmable On-Die Termination (ODT)

Programmable CAS Latency: 4, or 5

Differential/Redundant Data Strobe signals

SDRAM Addressing (Row/Col/Bank): 14/10/3

Fully RoHS Compliant

### Description

DTM63391B is an Unbuffered 128Mx72 memory module, which conforms to JEDEC's DDR2 standard. The DIMM has one Rank, comprised of nine 128Mx8 DDR2 Samsung SDRAMs. One 2K-bit EEPROM is used for Serial Presence Detect.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals.

The Data Strobe signals may be used either as differential pairs, or as single-ended strobes with the /DQS signals disabled.

Data Mask inputs are provided to selectively prevent data from being written to an 8-bit byte.

### Pin Configuration

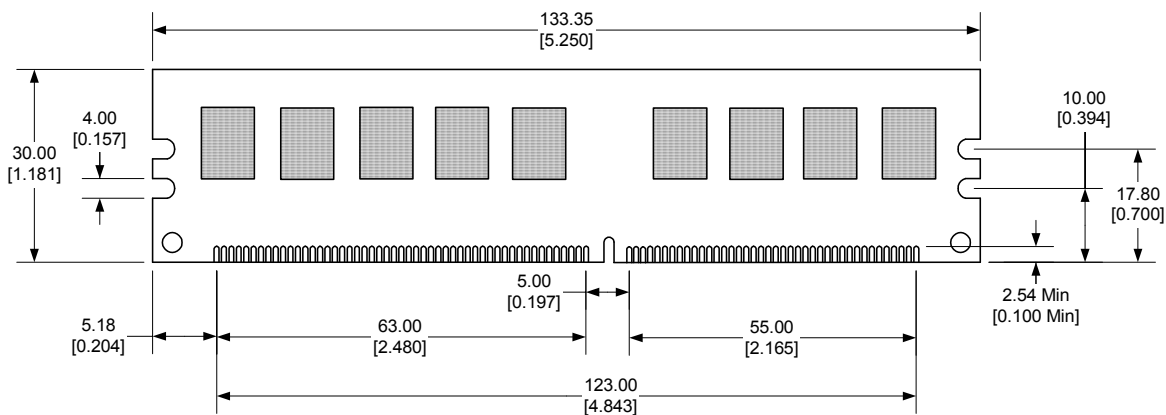
Front Side				Back Side			
1 VREF	31 DQ19	61 A4	91 VSS	121 VSS	151 VSS	181 VDD	211 DM5
2 VSS	32 VSS	62 VDD	92 /DQS5	122 DQ4	152 DQ28	182 A3	212 NC
3 DQ0	33 DQ24	63 A2	93 DQS5	123 DQ5	153 DQ29	183 A1	213 VSS
4 DQ1	34 DQ25	64 VDD	94 VSS	124 VSS	154 VSS	184 VDD	214 DQ46
5 VSS	35 VSS	65 VSS	95 DQ42	125 DM0	155 DM3	185 CK0	215 DQ47
6 /DQS0	36 /DQS3	66 VSS	96 DQ43	126 NC	156 NC	186 /CK0	216 VSS
7 DQS0	37 DQS3	67 VDD	97 VSS	127 VSS	157 VSS	187 VDD	217 DQ52
8 VSS	38 VSS	68 NC	98 DQ48	128 DQ6	158 DQ30	188 A0	218 DQ53
9 DQ2	39 DQ26	69 VDD	99 DQ49	129 DQ7	159 DQ31	189 VDD	219 VSS
10 DQ3	40 DQ27	70 A10	100 VSS	130 VSS	160 VSS	190 BA1	220 CK2
11 VSS	41 VSS	71 BA0	101 SA2	131 DQ12	161 CB4	191 VDD	221 /CK2
12 DQ8	42 CB0	72 VDD	102 NC	132 DQ13	162 CB5	192 /RAS	222 VSS
13 DQ9	43 CB1	73 /WE	103 VSS	133 VSS	163 VSS	193 /S0	223 DM6
14 VSS	44 VSS	74 /CAS	104 /DQS6	134 DM1	164 DM8	194 VDD	224 NC
15 /DQS1	45 /DQS8	75 VDD	105 DQS6	135 NC	165 NC	195 ODT0	225 VSS
16 DQS1	46 DQS8	76 NC	106 VSS	136 VSS	166 VSS	196 A13	226 DQ54
17 VSS	47 VSS	77 NC	107 DQ50	137 CK1	167 CB6	197 VDD	227 DQ55
18 NC	48 CB2	78 VDD	108 DQ51	138 /CK1	168 CB7	198 VSS	228 VSS
19 NC	49 CB3	79 VSS	109 VSS	139 VSS	169 VSS	199 DQ36	229 DQ60
20 VSS	50 VSS	80 DQ32	110 DQ56	140 DQ14	170 VDD	200 DQ37	230 DQ61
21 DQ10	51 VDD	81 DQ33	111 DQ57	141 DQ15	171 NC	201 VSS	231 VSS
22 DQ11	52 CKE0	82 VSS	112 VSS	142 VSS	172 VDD	202 DM4	232 DM7
23 VSS	53 VDD	83 /DQS4	113 /DQS7	143 DQ20	173 A15 *	203 NC	233 NC
24 DQ16	54 BA2	84 DQS4	114 DQS7	144 DQ21	174 A14 *	204 VSS	234 VSS
25 DQ17	55 NC	85 VSS	115 VSS	145 VSS	175 VDD	205 DQ38	235 DQ62
26 VSS	56 VDD	86 DQ34	116 DQ58	146 DM2	176 A12	206 DQ39	236 DQ63
27 /DQS2	57 A11	87 DQ35	117 DQ59	147 NC	177 A9	207 VSS	237 VSS
28 DQS2	58 A7	88 VSS	118 VSS	148 VSS	178 VDD	208 DQ44	238 VDDSPD
29 VSS	59 VDD	89 DQ40	119 SDA	149 DQ22	179 A8	209 DQ45	239 SA0
30 DQ18	60 A5	90 DQ41	120 SCL	150 DQ23	180 A6	210 VSS	240 SA1

\* Connected but not used

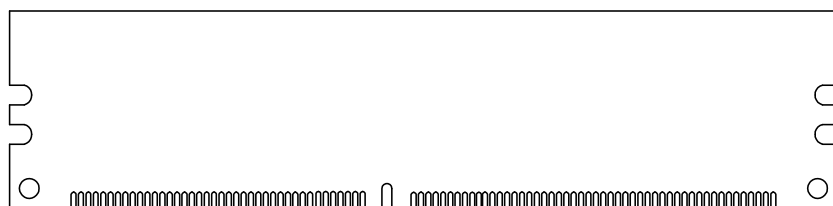
### Pin Description

Name	Function
CB[7:0]	Data Check Bits
DQ[63:0]	Data Bits
DQS[8:0], /DQS[8:0]	Differential Data Strobes
DM[8:0]	Data Mask
CK[2:0], /CK[2:0]	Differential Clock Inputs
CKE0	Clock Enables
/CAS	Column Address Strobe
/RAS	Row Address Strobe
/S0	Chip Selects
/WE	Write Enable
A[15:0]	Address Inputs
BA[2:0]	Bank Addresses
ODT0	On Die Termination Inputs
SA[2:0]	SPD Address
SCL	SPD Clock Input
SDA	SPD Data Input/Output
VSS	Ground
VDD	Power
VDDSPD	SPD EEPROM Power
VREF	Reference Voltage
NC	No Connection

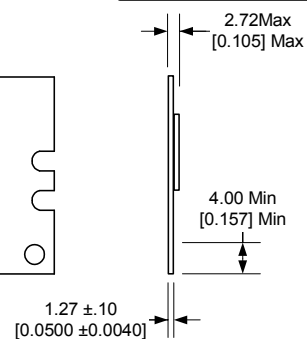
### Front view



### Back view



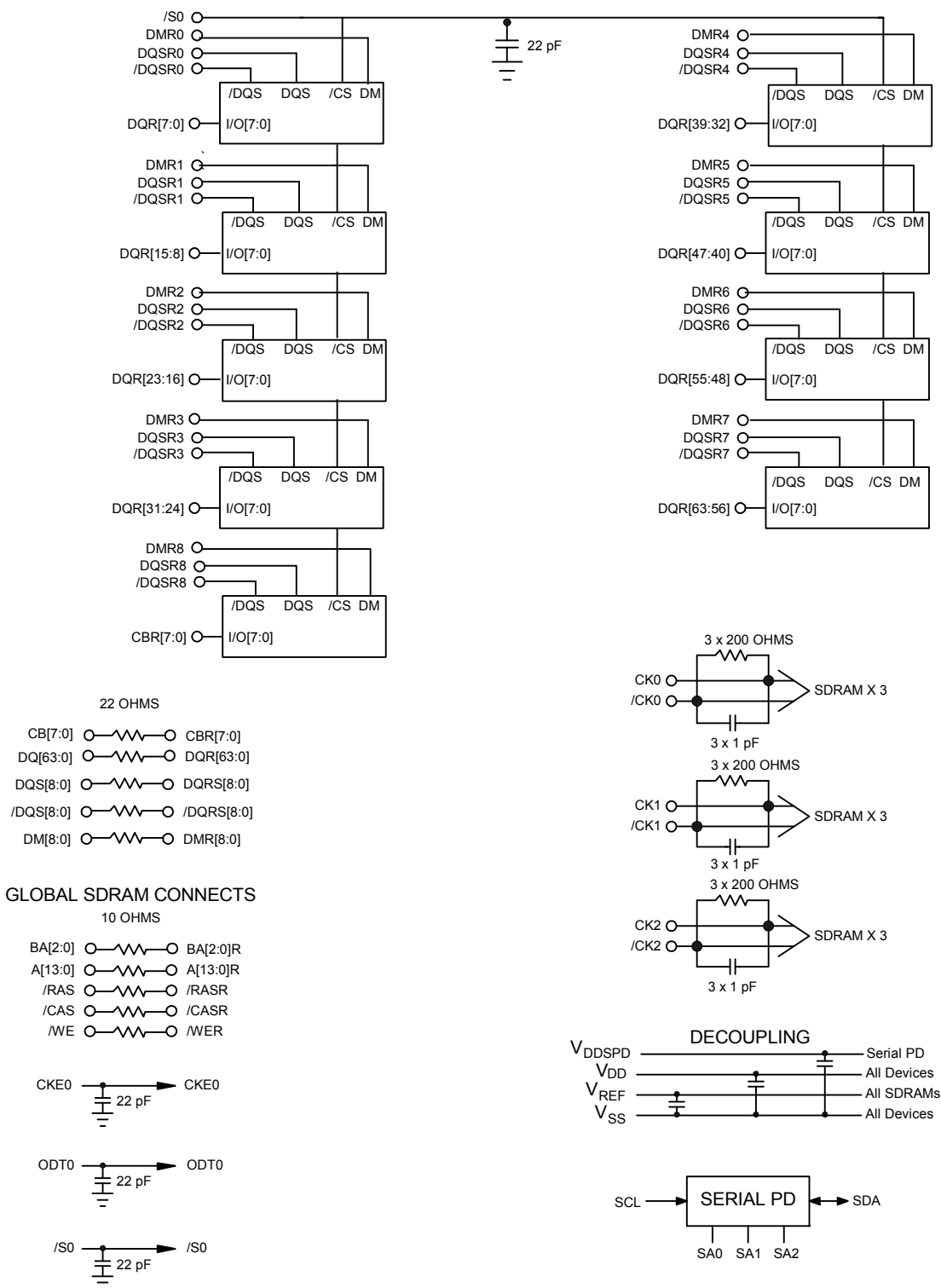
### Side view



### Notes

Tolerances on all dimensions except where otherwise indicated are  $\pm .13$  (.005).

All dimensions are expressed: millimeters [inches]



### Absolute Maximum Ratings

(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

PARAMETER	Symbol	Minimum	Maximum	Unit
Temperature, non-Operating	$T_{STORAGE}$	-55	100	C
Ambient Temperature, Operating	$T_A$	0	70	C
DRAM Case Temperature, Operating	$T_{CASE}$	0	95	C
Voltage on $V_{DD}$ relative to $V_{SS}$	$V_{DD}$	-0.5	2.3	V
Voltage on Any Pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5	2.3	V

Notes:

Temperature above 85C requires doubling the refresh rate i.e. 3.9us instead of 7.8us

### Recommended DC Operating Conditions ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Typical	Maximum	Unit	Note
Power Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V	
I/O Reference Voltage	$V_{REF}$	0.49 $V_{DD}$	0.50 $V_{DD}$	0.51 $V_{DD}$	V	1
Bus Termination Voltage	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V	

Notes:

- The value of  $V_{REF}$  is expected to equal one-half  $V_{DD}$  and to track variations in the  $V_{DD}$  DC level. Peak-to-peak noise on  $V_{REF}$  may not exceed  $\pm 1\%$  of its DC value.

### DC Input Logic Levels, Single-Ended ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(DC)}$	$V_{REF} + 0.125$	$V_{DD} + 0.300$	V
Logical Low (Logic 0)	$V_{IL(DC)}$	-0.300	$V_{REF} - 0.125$	V

### AC Input Logic Levels, Single-Ended ( $T_A = 0$ to 70 C, Voltage referenced to $V_{SS} = 0$ V)

PARAMETER	Symbol	Minimum	Maximum	Unit
Logical High (Logic 1)	$V_{IH(AC)}$	$V_{REF} + 0.250$	-	V
Logical Low (Logic 0)	$V_{IL(AC)}$	-	$V_{REF} - 0.250$	V

### Differential Input Logic Levels ( $T_A = 0$ to $70^\circ\text{C}$ , Voltage referenced to $V_{SS} = 0\text{ V}$ )

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
DC Input Signal Voltage	$V_{IN(DC)}$	-0.300	$V_{DD} + 0.300$	V	1
DC Differential Input Voltage	$V_{ID(DC)}$	-0.250	$V_{DD} + 0.600$	V	2
AC Differential Input Voltage	$V_{ID(AC)}$	-0.500	$V_{DD} + 0.600$	V	3
AC Differential Cross-Point Voltage	$V_{IX(AC)}$	$0.50 V_{DD} - 0.175$	$0.50 V_{DD} + 0.175$	V	4

Notes:

1.  $V_{IN(DC)}$  specifies the allowable DC excursion of each input of a differential pair.
2.  $V_{ID(DC)}$  specifies the input differential voltage, *i.e.* the absolute value of the difference between the two voltages of a differential pair.
3.  $V_{ID(AC)}$  specifies the input differential voltage required for switching.
4. The typical value of  $V_{IX(AC)}$  is expected to be  $0.5 V_{DD}$  and is expected to track variations in  $V_{DD}$ .

### Capacitance ( $T_A = 25^\circ\text{C}$ , $f = 100\text{ MHz}$ )

PARAMETER	Pin	Symbol	Minimum	Maximum	Unit
Input Capacitance, Clock	CK[2:0], /CK[2:0]	CIN1	3	6	pF
Input Capacitance, Address and Control	BA[1:0], A[13:0], /S0, /RAS, /CAS, /WE, CKE0, ODT0	CIN2	9	18	pF
Input/Output Capacitance	DQ[63:0], CB[7:0], DQS[8:0], /DQS[8:0], DM[8:0]	CIO	2.5	3.5	pF

### DC Characteristics ( $T_A = 0$ to $70^\circ\text{C}$ , Voltage referenced to $V_{SS} = 0\text{ V}$ )

PARAMETER	Symbol	Minimum	Maximum	Unit	Note
Input Leakage Current Command and Address	$I_{LI}$	-80	80	$\mu\text{A}$	1
Input Leakage Current S0, CKE0, ODT0	$I_{LI}$	-40	40	$\mu\text{A}$	1
Input Leakage Current CK[2:0], /CK[2:0]	$I_{LI}$	-30	30	$\mu\text{A}$	1
Input Leakage Current DM	$I_{LI}$	-10	10	$\mu\text{A}$	1
Output Leakage Current DQS, DQ	$I_{OZ}$	-10	10	$\mu\text{A}$	2
Output Minimum Source DC Current	$I_{OH}$	-13.4	-	mA	3
Output Minimum Sink DC Current	$I_{OL}$	+13.4	-	mA	4

Notes:

1. These values are guaranteed by design and are tested on a sample basis only
2. DQx and ODT are disabled, and  $0\text{ V} \leq V_{OUT} \leq V_{DD}$ .
3.  $V_{DD} = 1.7\text{ V}$ ,  $V_{OUT} = 1420\text{ mV}$ .  $(V_{OUT} - V_{DD})/I_{OH}$  must be less than 21 Ohms for values of  $V_{OUT}$  between  $V_{DD}$  and  $(V_{DD} - 280\text{ mV})$ .
4.  $V_{DD} = 1.7\text{ V}$ ,  $V_{OUT} = 280\text{ mV}$ .  $V_{OUT}/I_{OL}$  must be less than 21 Ohms for values of  $V_{OUT}$  between  $0\text{ V}$  and  $280\text{ mV}$ .

**I<sub>DD</sub> Specifications and Conditions** (T<sub>A</sub> = 0 to 70 °C, Voltage referenced to V<sub>SS</sub> = 0 V)

PARAMETER	Symbol	Test Condition	Max Value	Unit
Operating One Bank Active-Precharge Current	I <sub>DD0</sub>	CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching.	585	mA
Operating One Bank Active-Read-Precharge Current	I <sub>DD1</sub>	I <sub>OUT</sub> = 0 mA; BL = 4, CL = 5 ns, AL = 0; CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching.	675	mA
Precharge Power-Down Current	I <sub>DD2P</sub>	All banks idle; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating.	90	mA
Precharge Quiet Standby Current	I <sub>DD2Q</sub>	All banks idle; CKE is HIGH, /CS is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating.	243	mA
Precharge Standby Current	I <sub>DD2N</sub>	All banks idle; CKE is HIGH, /CS is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching.	315	mA
Active Power-Down Current	I <sub>DD3P</sub>	All banks open; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating. Fast Power-down exit (Mode Register bit 12 = 0)	180	mA
Active Power-Down Current	I <sub>DD3P</sub>	All banks open; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating. Slow Power-down exit (Mode Register bit 12 = 1)	108	mA
Active Standby Current	I <sub>DD3N</sub>	All banks open; t <sub>RAS</sub> = 70 ms; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching.	405	mA
Operating Burst Write Current	I <sub>DD4W</sub>	All banks open, Continuous burst writes; BL = 4, CL = 5 t <sub>CK</sub> , AL = 0; t <sub>RAS</sub> = 70 ms, CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching.	1125	mA
Operating Burst Read Current	I <sub>DD4R</sub>	All banks open, Continuous burst reads, I <sub>OUT</sub> = 0 mA; BL = 4, CL = 5 t <sub>CK</sub> , AL = 0, t <sub>RAS</sub> = 70 ms; CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching.	1125	mA
Burst Refresh Current	I <sub>DD5</sub>	Refresh command at every 75 ns; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching.	1485	mA
Self Refresh Current	I <sub>DD6</sub>	CK and /CK at 0 V; CKE ≤ 0.2 V; Other control and address bus inputs are floating; Data bus inputs are floating.	90	mA
Operating Bank Interleave Read Current	I <sub>DD7</sub>	All bank interleaving reads, I <sub>OUT</sub> = 0 mA; BL = 4, CL = 5 t <sub>CK</sub> ; AL = t <sub>RCD</sub> (IDD) - 1 × t <sub>CK</sub> (IDD); t <sub>RRD</sub> = 7.5 ns; CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching.	1575	mA

Note: For all I<sub>DDX</sub> measurements, t<sub>CK</sub> = 3.0 ns, t<sub>RC</sub> = 60 ns, t<sub>RCD</sub> = 15 ns, t<sub>RAS</sub> = 45 ns, and t<sub>RP</sub> = 15 ns unless otherwise specified. All currents are based on DRAM absolute maximum values.

### AC Operating Conditions

PARAMETER	Symbol	Min	Max	Unit
DQ Output Access Time from Clock	$t_{AC}$	-450	+450	ps
CAS-to-CAS Command Delay	$t_{CCD}$	2	-	$t_{CK}$
Clock High Level Width	$t_{CH}$	0.48	0.52	$t_{CK}$
Clock Cycle Time	$t_{CK}$	3000	8000	ps
Clock Low Level Width	$t_{CL}$	0.48	0.52	$t_{CK}$
Data Input Hold Time after DQS Strobe	$t_{DH}$	175	-	ps
DQ Input Pulse Width	$t_{DIPW}$	0.35	-	$t_{CK}$
DQS Output Access Time from Clock	$t_{DQSCK}$	-400	+400	ps
Write DQS High Level Width	$t_{DQSH}$	0.35	-	$t_{CK}$
Write DQS Low Level Width	$t_{DQSL}$	0.35	-	$t_{CK}$
DQS-Out Edge to Data-Out Edge Skew	$t_{DQSQ}$	240	-	ps
Data Input Setup Time Before DQS Strobe	$t_{DS}$	100	-	ps
DQS Falling Edge from Clock, Hold Time	$t_{DSH}$	0.2	-	$t_{CK}$
DQS Falling Edge to Clock, Setup Time	$t_{DSS}$	0.2	-	$t_{CK}$
Clock Half Period	$t_{HP}$	minimum of $t_{CH}$ or $t_{CL}$	-	ns
Address and Command Hold Time after Clock	$t_{IH}$	275	-	ps
Address and Command Setup Time before Clock	$t_{IS}$	200	-	ps
Load Mode Command Cycle Time	$t_{MRD}$	2	-	$t_{CK}$
DQ-to-DQS Hold	$t_{QH}$	$t_{HP} - t_{QHS}$	-	-
Data Hold Skew Factor	$t_{QHS}$	340	-	ps
Active-to-Precharge Time	$t_{RAS}$	45	70K	ns
Active-to-Active / Auto Refresh Time	$t_{RC}$	60	-	ns
RAS-to-CAS Delay	$t_{RCD}$	15	-	ns
Average Periodic Refresh Interval	$t_{REFI}$	-	7.8	$\mu$ s
Auto Refresh Row Cycle Time	$t_{RFC}$	127.5	-	ns
Row Precharge Time	$t_{RP}$	15	-	ns
Read DQS Preamble Time	$t_{RPRE}$	0.9	1.1	$t_{CK}$
Read DQS Postamble Time	$t_{RPST}$	0.4	0.6	$t_{CK}$
Row Active to Row Active Delay	$t_{RRD}$	7.5	-	ns
Internal Read to Precharge Command Delay	$t_{RTP}$	7.5	-	ns
Write DQS Preamble Time	$t_{WPRE}$	0.35	-	ps
Write DQS Postamble Time	$t_{WPST}$	0.4	0.6	$t_{CK}$
Write Recovery Time	$t_{WR}$	15	-	ns
Internal Write to Read Command Delay	$t_{WTR}$	7.5	-	ns
Exit Self Refresh to Non-Read Command	$t_{XSNR}$	$t_{RFC}(\text{min}) + 10$	-	ns
Exit Self Refresh to Read Command	$t_{XSRD}$	200	-	$t_{CK}$

### SERIAL PRESENCE DETECT MATRIX

Byte#	Function.	Value	Hex
0	Number of Bytes Utilized by Module Manufacturer	128 bytes	0x80
1	Total number of Bytes in Serial PD device	256 bytes	0x08
2	Memory Type	DDR2 SDRAM	0x08
3	Number of Row Addresses	14	0x0E
4	Number of Column Addresses	10	0x0A
5	Module Attributes - Number of Ranks, Package and Height		0x60
	# of Ranks -	1	
	Card on Card -	No	
	DRAM Package -	Planar	
	Module Height -	30mm	
6	Module Data Width.	72	0x48
7	Reserved	UNUSED	0x00
8	Voltage Interface Level of this assembly	SSTL/1.8V	0x05
9	SDRAM Cycle time. (Max. Supported CAS Latency). CL=X (tCK) ns	3	0x30
10	SDRAM Access from Clock. (Highest CAS latency). (tAC) ns	0.45	0x45
11	DIMM configuration type (Non-parity, Parity or ECC)		0x02
	Data Parity -		
	Data ECC -	X	
	Address/Command Parity -		
	TBD -		
	TBD -		
	TBD -		
	TBD -		
	TBD -		
12	Refresh Rate/Type (us)	7.8 (SR)	0x82
13	Primary SDRAM Width	8	0x08
14	Error Checking SDRAM Width	8	0x08
15	Reserved	UNUSED	0x00
16	SDRAM Device Attributes: Burst Lengths Supported		0x0C
	TBD -		
	TBD -		
	Burst Length = 4 -	X	
	Burst Length = 8 -	X	
	TBD -		
	TBD -		
	TBD -		
	TBD -		
17	SDRAM Device Attributes - Number of Banks on SDRAM Device	8	0x08
18	SDRAM Device Attributes: CAS Latency		0x30
	TBD -		
	TBD -		



	Latency = 2 -			
	Latency = 3 -			
	Latency = 4 -	X		
	Latency = 5 -	X		
	Latency = 6 -			
	TBD -			
19	DIMM Mechanical Characteristics. Max. module thickness. (mm)	x <= 4.10	0x01	
20	DIMM type information		0x02	
	Regular RDIMM (133.35mm) -			
	Regular UDIMM (133.35mm) -	X		
	SODIMM (67.6mm) -			
	Micro-DIMM (45.5mm) -			
	Mini RDIMM (82.0mm) -			
	Mini UDIMM (82.0mm) -			
	TBD -			
21	SDRAM Module Attributes (Refer to Byte20 for DIMM type information).		0x00	
	Number of active registers on the DIMM (N/A for UDIMM) -			1
	Number of PLL on the DIMM (N/A for UDIMM) -			0
	FET Switch External Enable -			No
	TBD -			
	Analysis probe installed -			No
	TBD -			
22	SDRAM Device Attributes: General		0x03	
	Includes Weak Driver -			X
	Supports 50 ohm ODT -			X
	Supports PASR (Partial Array Self Refresh) -			
	TBD -			
	TBD -			
	TBD -			
	TBD -			
23	Minimum Clock Cycle Time at Reduced CAS Latency, CL = X-1 (ns)	3.75	0x3D	
24	Maximum Data Access Time (tAC ) from Clock at CL = X- 1 (ns)	0.45	0x45	
25	Minimum Clock Cycle Time at CL = X-2 (ns)	UNUSED	0x00	
26	Maximum Data Access Time (tAC ) from Clock at CL = X-2 (ns)	UNUSED	0x00	
27	Minimum Row Precharge Time (tRP ) (ns)	15	0x3C	
28	Minimum Row Active to Row Active Delay (tRRD ) (ns)	7.5	0x1E	
29	Minimum RAS to CAS Delay (tRCD ) (ns)	15	0x3C	
30	Minimum Active to Precharge Time (tRAS ) (ns)	45	0x2D	
31	Module Rank Density	1GB	0x01	
32	Address and Command Setup Time Before Clock (tIS) (ns)	0.2	0x20	
33	Address and Command Hold Time After Clock (tIH) (ns)	0.27	0x27	
34	Data Input Setup Time Before Strobe (tDS) (ns)	0.1	0x10	
35	Data Input Hold Time After Strobe (tDH) (ns)	0.17	0x17	

36	Write Recovery Time (tWR) (ns)	15	0x3C
37	Internal write to read command delay (tWTR) (ns)	7.5	0x1E
38	Internal read to precharge command delay (tRTP) (ns)	7.5	0x1E
39	Memory Analysis Probe Characteristics.	UNUSED	0x00
40	Extension of Byte 41(tRC) and Byte 42 (tRFC) (ns)		0x06
	Add this value to byte 41 -	0	
	Add this value to byte 42 -	0.5	
41	SDRAM Device Minimum Active to Active/Auto Refresh Time (tRC) (ns)	60	0x3C
42	SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC). (ns)	127.5	0x7F
43	SDRAM Device Maximum Cycle Time (tCK max). (ns)	8	0x80
44	SDRAM Dev DQS-DQ Skew for DQS & DQ signals (tDQSQ) (ns)	0.24	0x18
45	DDR SDRAM Device Read Data Hold Skew Factor (tQHS) (ns)	0.34	0x22
46	PLL Relock Time (us)	UNUSED	0x00
47	DRAM maximum Case Temperature Delta. (Degree C).		0x51
	DT4R4W Delta (Bits 0:3) -	0.4	
	Tcasemax delta (Bits 7:4) -	10	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi T-A DRAM). (C/Watt)	58	0x74
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/ Mode Bits (DT0/Mode Bits). (Degree C).		0x57
	Bit 0. If "0" DRAM does not support high temperature self-refresh entry -	1	
	Bit 1. If "0" Do not need double refresh rate for the proper operation -	1	
	DT0, (Bits 2:7) -	6.3	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q). (Degree C).	6	0x3C
51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down (DT2P). (Degree C).	1.44	0x60
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N). (Degree C).	6.9	0x2E
53	DRAM Case temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast). (Degree C).	4.4	0x58
54	DRAM Case temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow). (Degree C).	2.2	0x58
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit). (Degree C).		0x4A
	Bit 0. "0" if DT4W is greater than DT4R -	0	
	DT4R, ( Bits 1:7 ) -	14.8	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (DT5B). (Degree C).	24.5	0x31

57	DRAM Case Temperature Rise from Ambient due to Bank Interleave Reads with Auto-Precharge (DT7). (Degree C).	26.5	0x35
58	Thermal Resistance of PLL Package from Top to Ambient (Psi T-A PLL). (C/Watt).	UNUSED	0x00
59	Thermal Resistance of Register Package from Top to Ambient ( Psi T-A Register). (C/Watt).	UNUSED	0x00
60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active). (Degree C).	UNUSED	0x00
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit).		0x00
	Bit 0.If "0"Unit for Bits 2:7 is 0.75C -	0.75	
	Bit 1. RFU. Default: 0 -	0	
	Register Active,( Bits 2:7 ) -	0	
62	SPD Revision	Revision 1.2	0x12
63	Checksum for Bytes 0-62		0xA7
64	Module Manufacturer's JEDEC ID Code	Dataram ID	0x7F
65	Module Manufacturer's JEDEC ID Code	Dataram ID	0x91
66-71	Module Manufacturer's JEDEC ID Code	UNUSED	0x00
72	Module Manufacturing Location	UNUSED	0x00
73-90	Module Part Number		0x20
91, 92	Module Revision Code	UNUSED	0x00
93, 94	Module Manufacturing Date	UNUSED	0x00
95	Module Serial Number	S	0x53
96	Module Serial Number	E	0x45
97	Module Serial Number	R	0x52
98	Module Serial Number	#	0x23
99-127	Manufacturer's Specific Data	UNUSED	0x00



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